REMARKS

Claims 1-27 are pending. Claims 5, 10, 12, 13, and 21 were rejected due to informalities. Claims 5, 10, 11, 13, and 21 have been amended to correct informalities. The antecedent basis rejection of claim 12 is believed overcome due to the amendment to claim 10. The Examiner objected to the term "substantial" in claims 1, 17, and 25. The term "substantial" has been removed from claim 1, 17, and 25 to overcome this objection.

The Examiner rejected claims 1-27 under 35 U.S.C. 101 because the Examiner argues that the claimed invention is directed to non-statutory subject matter. The Examiner argues that claims 1-16 are software per se and claims 1-27 do not produce a tangible result. The Applicants respectfully disagree with the Examiner's rejection.

It is noted that the Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility (2005-10-26) states: In determining whether the claim is for a "practical application," the focus is not on whether the steps taken to achieve a particular result are useful, tangible and concrete, but rather that the final result is "useful, tangible and concrete." The Federal Circuit has provided further guidance in distinguishing between the judicially-created exceptions to patentable subject matter and eligible subject matter. The focus of the inquiry is whether the claim, considered as a whole, constitutes "a practical application of an abstract idea." State Street, 149 F.3d at 1373, 47 USPQ2d at 1600.

Taken as a whole, the independent claims are directed at generating multiple test designs. Generating each design includes instantiating an I/O structure, parameterizing multiple submodules, and providing interconnect logic. It is submitted that, taken as a whole, the independent claims provide a useful, tangible and concrete result in generated test designs that allow testing of design automation tools. Consequently, the non-statutory subject matter rejection is believed overcome.

The Examiner reject independent claims 1, 17, and 25 under 35 U.S.C. 103(a) as being unpatentable over Zaidi (USPAP 2002/0038401) in view of Heinkel (USPAP 2004/0015739). However, Zaidi and Heinkel, even if appropriately combined, do not teach or suggest generating a plurality of test designs.

The Examiner argues that Zaidi describes generating multiple test designs in paragraph [0037]. The Applicants respectfully disagree. Zaidi describes in paragraph [0037]. "Most of the block design directories containing RTL source code have a separate subdirectory structure underneath, e.g., "cpubr/", "cpumem/", "dma/", "intctl/", "lcd/", "mc/", "palmbus/", "pio/", "sysctl/", "timer/", and "uart/". The "<block>/sim/" subdirectory includes the simulation tests for the design. The "<block>/synop/" subdirectory includes the Synopsys synthesis scripts and output files for the design. The "<block>/vlog/" subdirectory includes the Verilog RTL source code for the design; if the embodiment language were VHDL, the "<block>/vhdl/" subdirectory includes the VHDL RTL source code for the design."

Paragraph [0037] only describes where the source code for particular components is located. The Zaidi paragraph [0037] does not teach or suggest anything about generating multiple designs or generating test designs.

The Examiner also argues that Heinkel teaches generating multiple test designs in paragraphs [0057] - [0060]. However, paragraphs [0057] – [0060] only describes a single "device under test 50." Heinkel in fact does not teach generating a plurality of test designs because Heinkel is configured to test a single DUT such as a single ASIC.

By contrast, various embodiments of the present invention allow generation of multiple test designs to allow testing of a design automation tool. In one example, a test design can include a processor, a DSP core, a timer, and a network interface while another generated test design includes a processor, a cyprographic core, and a PIO, and a network interface. Top level modules are instantiated, submodules are parameterized, and interconnection logic is provided for each generated test design. It is respectfully submitted that neither Heinkel nor Zaidi teach or suggest these elements recited in the independent claims.

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicants believe that all pending claims are allowable in their present form. Please feel free to contact the undersigned at the number provided below if there are any questions, concerns, or remaining issues.

Respectfully submitted,
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